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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/074,537	02/12/2002	Shahla Khorram	BP 2133	7244

7590 02/01/2006  
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EXAMINER

NGUYEN, DUC M

ART UNIT PAPER NUMBER

2685

DATE MAILED: 02/01/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

10/074,537

Applicant(s)

KHORRAM, SHAHLA

Examiner

Duc M. Nguyen

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 30 November 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-18 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-18 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

### DETAILED ACTION

This action is in response to applicant's response filed on 11/30/05. Claims 1-18 are now pending in the present application.

#### *Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims **1-5, 16-18** are rejected under 35 U.S.C. 103(a) as being unpatentable by **Weber** (US **6,504,433**) in view of **Yamaguchi** (US Patent Number **6,804,500**) and **Vathulya** (US Patent Number **6,636,119**).

Regarding claim **1**, **Weber** discloses a highly linear power amplifier comprises :

- a component (see the inductor in Fig. 1);
- first transistor pair coupled in series with the component, wherein a first transistor (12) of the first transistor pair is coupled to receive an input signal and wherein a second transistor (14) of the first transistor pair is coupled to receive a first enable signal ( $V_{DD}$ ); wherein it is clear that the transistor pair would provide a first gain with linearity as claimed (see col. 2, lines 18-20).

However, **Weber** fails to disclose a second transistor pair coupled in parallel with the first transistor pair. However, **Yamaguchi** discloses an amplifier wherein the

amplifier is formed by three amplifier blocks coupled in parallel, each block having a difference enable signal  $V_{cnt}$  and a difference output gain (see Fig. 12 and col. 10, line 28 – col. 11, line 22), for improving wide dynamic range of the amplifier. Since using multiple amplifiers for increasing gain margin while retaining linearity is well known in the art, it would have been obvious to one skilled in the art at the time the invention was made to provide the above teachings of Yamaguchi to Weber for providing a second transistor pair coupled in parallel to the first transistor pair, in the similar way as illustrated by **Vanthulya** in Figs. 3-4, thereby result in a second transistor pair with a second linearity gain as claimed, for increasing the gain margin of the power amplifier while retaining its linearity characteristic.

Regarding claim **16**, the claim is rejected for the same reason as set forth in claim 1 above, wherein it would have been obvious to one skilled in the art at the time the invention was made to replace the single-ended amplifier (Fig. 1 of Weber) with the differential amplifier (see Fig. 7 of Weber regarding I-Q components) as well and would work equally well, for utilizing advantages of differential signals such as low noise figure (i.e, noises tends to cancel out when combining differential signals).

Regarding claim **2**, the claim is rejected for the same reason as set forth in claim 1 above. In addition, **Weber** discloses the component comprise at least one resistor or inductor as claimed (see Fig. 1).

Regarding claim **3**, the claim is rejected for the same reason as set forth in claim 1 above. In addition, since Yamaguchi also discloses a third amplifier block, it is clear that Weber as modified would disclose at least one other transistor pair as claimed, for

further increasing the gain margin of the amplifier.

Regarding claim **4**, the claim is rejected for the same reason as set forth in claim 1 above. In addition, since **Yamaguchi** discloses high, medium and low output amplifier cell block (see col. 10, lines 28-37) and that a gain of a transistor is proportional to its size (see col. 17, lines 20-23), it is clear that Weber and Yamaguchi as modified would disclose the first gain is greater than the second gain, and the first size is greater than the second size with a ratio as claimed.

Regarding claim **5**, the claim is interpreted and rejected for the same reason as set forth in claim 16 above, wherein it is clear that the differential transistor pair would comprise a first complimentary and second complimentary transistor pair as claimed.

Regarding claims **17-18**, the claims are interpreted and rejected for the same reason as set forth in claim **5** above, wherein it is clear that the differential transistor pair would comprise p-channel or n-channel transistor as claimed (see Weber, col. 9, lines 58-60).

3. Claims **6-15** are rejected under 35 U.S.C. 103(a) as being unpatentable by **Weber** in view of **Yamaguchi** and **Vathulya**, and further in view of **Hans** (US Patent Number **5,923,215**).

Regarding claim **6**, the claim is rejected for the same reason as set forth in claim 1 above. In addition, Yamaguchi discloses a control module to generate the first and second control (or enable) signals (see col. 12, lines 51-59). However, Yamaguchi fails to disclose the control signal is based on desired output levels of the amplifier.

However, such control signal based on desired output levels of the amplifier is well

known in the art as disclosed by Hans (see Fig. 1). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to further incorporate the above teaching of Hans to Weber and Yamaguchi for providing control signals based on desired output levels of the amplifier as claimed, for controlling output power in order to minimize interferences, or reduce power consumption.

Regarding claim 7, the claim is interpreted and rejected for the same reason as set forth in claims 4 and 6 above, wherein it is clear that the cumulative gain is a combination of two gains and thus would be greater than either the first gain or the second gain.

Regarding claim 8, the claim is rejected for the same reason as set forth in claims 1, 6 above. In addition, Yamaguchi discloses an upconverter (see Fig. 20A, ref. 106 regarding the modulator) and that it would have been obvious to one skilled in the art to utilize I-Q components (also known as differential signals) for IF signal as claimed, for utilizing advantages of differential signals such as low noise figure (i.e., noises tend to cancel out when combining differential signals).

Regarding claims 9-15, the claims are interpreted and rejected for the same reason as set forth in claim 8 above. In addition, since Yamaguchi also discloses a third amplifier block, it is clear that Weber and Yamaguchi as modified would disclose at least one other transistor pair as claimed, for further widening dynamic range of the amplifier. Further, it would have been obvious to one skilled in the art at the time the invention was made to replace the single-ended amplifier (Fig. 1 of Weber) with the differential amplifier (Fig. 2 of Weber) as well and would work equally well, for utilizing advantages

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of differential signals such as low noise figure (i.e, noises tends to cancel out when combining differential signals).

***Response to Arguments***

4. Applicant's arguments with respect to claims 1-18 have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

5. **Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks

Washington, D.C. 20231

**or faxed to:**

(571) 273-8300 (for formal communications intended for entry)

(571)-273-7893 (for informal or draft communications).

Hand-delivered responses should be brought to Customer Service Window,  
Randolph Building, 401 Dulany Street, Alexandria, VA 22314.

Any inquiry concerning this communication or communications from the examiner  
should be directed to Duc M. Nguyen whose telephone number is (571) 272-7893,  
Monday-Thursday (9:00 AM - 5:00 PM).

Or to Edward Urban (Supervisor) whose telephone number is (571) 272-7899.

Duc M. Nguyen

Jan 8, 2005

